Homework 2: 100 Points

This Homework focusses on Instruction Set Architecture, its principles and attributes.

Please submit your answers in an MS Word document or PDF and upload it in Canvas by the due date. There is a10% penalty per day for late submission without valid excuse.

Present your work neat, clear, organized, logical, and make your case; don’t leave it to our interpretation of your answer.

1. (30 Points) Consider the code sequence:

C= A + B

D= A-E

F= C+ D

Assume the values A, B, C, D, E, and F reside in memory. For each Architecture

1. (10 Points) Accumulator Architecture
2. (10 Points) Memory- Register Architecture
3. (10 Points) Register-Register Architecture

write the code assuming the instruction codes (opcode) are 8 bits, memory addresses are 32 bits, and register addresses are 6 bits and CPU has 64 Registers; and create a table which specifies:

* + The execution sequence
  + The variables that were destroyed in the course of execution
  + The overhead instruction just to overcome the loss of data
  + Total code size
  + The number of bytes of instruction and data moved to or from memory
  + The number of overhead data bytes.

1. (15 Points) Consider the C++ struct:

Struct foo {

char a;

bool b;

int c;

double d;

short e;

float f;

double g;

char \*cptr

float \*fptr;

int x;

};

1. (5 Points) What is the size of foo struct?
2. (5 Points) What is the memory size required?
3. (5 Points) What is the minimum memory size required if you re-arrange the struct?

Assume the following data type and sizes for the above struct in a 64-bit machine.

|  |  |
| --- | --- |
| **Data Type** | **Data size on 64-bit**  **machine (bytes)** |
| Char | 1 |
| Bool | 1 |
| Int | 4 |
| Long | 8 |
| Double | 8 |
| Short | 2 |
| Float | 4 |
| pointer | 8 |

1. (10 Points) Assume the following instruction mix for a RISC-V like RISC Program:
   * 15% of instructions are store
   * 25% of instructions are load
   * 15% of instructions are branches
   * 35% of instructions are integer arithmetic /logical
   * %5 of instructions are floating points
   * The rest of instructions (shift, move, etc.) are like arithmetic/logical instructions.

Further assume that:

* + Load and store instructions take 4 cycles each, branches take 3 cycles, arithmetic/logical instruction (and their likes) each takes one cycle, and floating point instructions take 12 cycles.

Compute the overall CPI of this RISC Program.

1. (20 Points) Write the following code in RISC-V. Assume A, B, C, and D are DP (Double–Precision) floating points, I and J are integers. Include comments on each line.

C = A – B

D = 2- A + B

If I = J then A=A+B; else B=B-A

1. (25 Points) Consider the code segment

for (i=0; i<=100; i++)

X[i] = X[i] + d

Assume X is an array of 64-bit integer, d is a 64-bit integer, and i is a 32-bit integer.

Assume X[0] is at address 0(x0) in memory, X[1] at x0 + 8, X[2] at x0 + 16, etc.

1. (15 Points) Write the code in RISC-V; include comments on each line.
2. (5 Points) What is the size of the RISC-V code in bytes?
3. (5 Points) What is the RISC-V code CPI? Assume Load and store instructions take 4 cycles each, branches take 3 cycles, and arithmetic/logical instruction each takes one cycle.